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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,389	10/23/2001	Niall Ffrench	PD-201155	2138

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/053,389	Applicant(s) FFRENCH ET AL.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) *23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 23 and 24 should be renumbered 24 and 25, respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10, 11, 16 and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams (US 5993055), ISSUED: November 30, 1999.

Regarding independent Claims 1 and 16, Williams discloses an Integrated Circuit (IC), comprising:

A plurality of modules, such as three identical processing sets (10, 11, 12) as shown in FIG. 1.

A scan chain combiner, such as fault detector unit (voter) 17 coupled to the outputs of three identical processing sets (10, 11, 12) for selecting one value per scan

chain received from the processing sets (10, 11, 12), where the value is indicative of errors in any of the processing sets (10, 11, 12). If the processing sets (10, 11, 12) are operating correctly, then they produce identical matching outputs to the voter 17, and the voter passes commands to an input/output (I/O) subsystem 18 for action. If, however, the outputs differ, then the voter causes corrective action by notifying an operator, via fault signal line 14 for the "change me" light (not shown) to be illuminated on the faulty processing set, to replace the defective processing set with a correctly functioning unit.

An output test (subsystem 18) for communicating the value from the fault detector unit (voter) 17 to an outside tester via JTAG test ports for checking the function and connections of the pins in circuit.

With respect to claimed limitation of an output test mux for communicating the value to a tester, the fault detector unit (voter) 17 performs the equivalent selection function of a mux, by identifying the defective processing set, out of the three processing sets (10, 11, 12) and then supplying a signal via line 14 to a processing set showing a fault to cause a "change me" light (not shown) to be illuminated on the faulty processing set.

Regarding Claims 4 and 20-23, Williams discloses a scan chain combiner voter (17), which utilizes majority voting logic for selecting the faulty processing set by comparing the outputs of each one of the modules processing sets (10, 11, 12) to each other. In the example shown, a defective processing set can normally be easily

identified by majority voting because of the two-to-one vote that will occur if one processing set fails or develops a temporary or permanent fault.

Regarding Claims 2, 3 and 11, Williams discloses FIG. 8, which shows a conventional chip 80 including a plurality of chip inputs (88) for receiving test signals from the tester (JTAG) via test port 84, wherein the test signals include test vectors and wherein the test vectors are processed in parallel by the processing sets (10, 11, 12).

Regarding Claim 5, Williams discloses processing sets (10, 11, 12) including a signature generator (74, FIG. 7), which comprises a plurality of parallel input linear feedback shift registers (40, FIG. 5) connected to a respective bit of the output from one of the element modules M0-M3 of the processing set (10, 11 or 12).

Regarding Claims 6-8, Williams discloses scan chain inputs of EXOR gate 46 for performing scan testing on the Integrated Circuit, wherein the scan chain inputs are coupled to a plurality of pins corresponding to a respective bit of the output from one of the modules M0-M3 of the processing set 10, 11 or 12.

Regarding Claims 10 and 19, Williams discloses FIG. 8 showing a conventional Integrated Circuit chip 80, which is an Application Specific Integrated Circuit (ASIC).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 12-15, 17, 18, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 5993055).

Regarding Claim 9, Williams does not explicitly disclose input muxes for communicating a specific module input signal to a respective module. However, Williams substantially discloses an internal bus IB for exchanging data among all processing modules, FIG. 4. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an internal bus IB and to communicate data to individual modules through the I/O module IOM as taught by Williams, without the need of additional switching logic for selecting a specific module.

Regarding Claims 12-15, 17,18, 24 and 25, Williams does not explicitly disclose an output mux for dynamically selecting an output from one of the modules to communicate to the rest of the logic for performing the design specific operation, wherein the output mux includes a scan module select signal for selecting specific scan outputs from one of the N modules, and wherein the output mux includes a scan mode signal for informing each one the registers that it will be tested. However, Williams substantially discloses a fault detector unit (voter) 17 for monitoring the operation of each of the processing sets (10, 11, 12) coupled to the logic analyzers LA. If a defective condition exists, then the output of the signature comparison circuit 62, located in the fault detector unit (voter) 17, triggers the logic analyzers 76, which identifies the faulty processing set. It would have been obvious to a person having

ordinary skill in the art at the time the invention was made to use fault detector unit (voter) 17, as taught by Williams, without having to add unnecessary output switching logic for selecting a specific faulty module.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 21 April 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner